3-8-00

*A*

# UTILITY PATENT APPLICATION TRANSMITTAL
## (Large Entity)
*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

| Docket No. |
|---|
| **BUR990238US1** |

| Total Pages in this Submission |
|---|
| 3 |

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

> STATISTICAL GUARDBAND METHODOLOGY

and invented by:

> Bilak et al.

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation**   ☐ **Divisional**   ☐ **Continuation-in-part (CIP)**   of prior application No.: _____

Which is a:

☐ **Continuation**   ☐ **Divisional**   ☐ **Continuation-in-part (CIP)**   of prior application No.: _____

Which is a:

☐ **Continuation**   ☐ **Divisional**   ☐ **Continuation-in-part (CIP)**   of prior application No.: _____

Enclosed are:

### Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having _____11_____ pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☐ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

P01ULRG/REV04

## Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*

   a. ☒ Formal        Number of Sheets      **4**

   b. ❏ Informal       Number of Sheets

4. ☒ Oath or Declaration

   a. ☒ Newly executed *(original or copy)*    ❏ Unexecuted

   b. ❏ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*

   c. ☒ With Power of Attorney    ❏ Without Power of Attorney

   d. ❏ *DELETION OF INVENTOR(S)*
       Signed statement attached deleting inventor(s) named in the prior application,
       see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ❏ Incorporation By Reference *(usable if Box 4b is checked)*
    The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ❏ Computer Program in Microfiche *(Appendix)*

7. ❏ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*

   a. ❏ Paper Copy

   b. ❏ Computer Readable Copy *(identical to computer copy)*

   c. ❏ Statement Verifying Identical Paper and Computer Readable Copy

## Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☒ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ❏ English Translation Document *(if applicable)*

11. ❏ Information Disclosure Statement/PTO-1449    ❏ Copies of IDS Citations

12. ❏ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing

     ❏ First Class    ☒ Express Mail *(Specify Label No.):* EL046031976US

## UTILITY PATENT APPLICATION TRANSMITTAL
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| Total Pages in this Submission |
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| **3** |

### Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
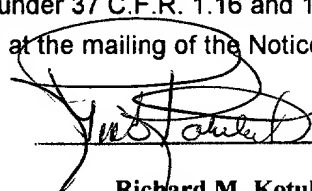
16. ☐ Additional Enclosures *(please identify below):*

### Fee Calculation and Transmittal

#### CLAIMS AS FILED

| For | #Filed | #Allowed | #Extra | Rate | Fee |
| --- | --- | --- | --- | --- | --- |
| Total Claims | 27 | - 20 = | 7 | x $18.00 | $126.00 |
| Indep. Claims | 3 | - 3 = | 0 | x $78.00 | $0.00 |
| Multiple Dependent Claims (check if applicable) ☐ | | | | | $0.00 |
| | | | | **BASIC FEE** | $690.00 |
| OTHER FEE *(specify purpose)* | | | | | |
| | | | | **TOTAL FILING FEE** | $816.00 |

☐ A check in the amount of _____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No.      09-0456
as described below. A duplicate copy of this sheet is enclosed.

    ☒ Charge the amount of      **$816.00**      as filing fee.

    ☒ Credit any overpayment.

    ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

    ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance,
    pursuant to 37 C.F.R. 1.311(b).

_____
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P01ULRG/REV04

# STATISTICAL GUARDBAND METHODOLOGY

5 ## Field of the Invention

This invention relates to methods and systems used to develop guardbands for assessing product specifications. More particularly it relates to methods and systems for developing guardbands for integrated circuits such as processors which are subject to manufacturing, testing

10 and environmental performance variations.

## Background of the Invention

Guardbands are typically used in manufacturing to protect against product and process
15 specification variations. However, if a manufacturer is too conservative in setting the guardband the amount of good products that fail testing is increased. If the guardband is too narrow, the products that go to customers may not function as specified. Two articles that discuss guardbands and the tradeoffs due to guardband placement are *The Economics of Guardband Placement*, Richard Williams and Charles Hawkins, International Test Conference 1993 and *The*
20 *Effect of Guardbands on Errors in Production Testing*, Richard Williams and Charles Hawkins, International Test Conference 1993.

Products, especially, integrated circuits, are designed to be used in a number of applications. Each application often provides a somewhat different set of operating conditions. To insure that the product can work in each of these applications, manufacturing tests must be
25 created to test both for these operating components and the surrounding impact of system components. This could involve a number of variables and parameters. One of the most important variables for processors is the speed which the processor operates in its system environment. Semiconductor manufacturers are constantly changing their designs, application conditions and processes to get faster processors.
30 Guardbands are determined today in a variety of ways. The easiest approach in developing guardbands is to develop tests that provide for the worst case of every variable. Other approaches include incorporating one of the variables mentioned above (usually test related variables) into determining a guardband, guardbanding reliability wear out mechanisms only, choosing a guardband to satisfy yield targets or not using a guardband at all. For many products,
35 especially integrated circuits that are processors, establishing a guardband using these approaches can lead to sub optimal results.

40

## Summary of the Invention

Current approaches of setting the same guardband across speed sorts, guardbanding to worst case application conditions, and ignoring other variables, ends up lowering yields, providing fewer high frequency integrated circuits, and more lower frequency circuits. It is an object of this invention to provide a method of establishing a product specification guardband that treats variables statistically and allows risk level to dictate the appropriate guardbands.

This invention is a method and system for determining product specification guardbands that first develops models of each variable that influences the product specification, such as: test environment, the test environment to system environment differences, system environment and reliability by incorporating these variables into a statistical representation of each. The models are then input into a statistical program which performs a Monte Carlo analysis or analytical analysis (by convolving statistical distributions) to determine the correct specification guardbands.

## Brief Description of the Drawings

FIG. 1 is a performance-distribution plot of an integrated circuit.

FIG. 2 is an example of the output which the guardband determines.

FIG. 3 is a flowchart illustrating the process for obtaining the model for the system environment.

FIG. 4 is a flowchart illustrating how the system to tester offset is generated.

FIG. 5 is a graph illustrating the distribution of various sample sizes.

FIG. 6 is a graph illustrating the fail rates due to reliability effects.

FIG. 7 is a flowchart illustrating the steps for determining a product guardband according to this invention.

FIG. 8 is a diagram that illustrates the typical hardware system used in determining the guardband.

## Description of Preferred Embodiment(s)

Determining final product specification guardbands are often the least considered items of product development. Yet the guardbands chosen can, and often do, have a major effect on product quality, revenue and yield. This is especially true when "deep sorts" exist. See the upper tail of the product performance-distribution plot of FIG 1. Many factors compound the deep sort guardband complexity, and guardband choice may eliminate sort based on small area at tail 2 of the distribution. A slight change in guardband can affect a large portion of parts due to large area under performance distribution curve of FIG. 1. Yet customers desire the highest performing parts. Slower performing parts are usually less susceptible to reliability mechanisms.

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This invention incorporates market sector tolerance targets ( quality and reliability) and models representing key variables that affect the product in the target market sector. It then uses these factors to produce a final product specification guardband using a Monte Carlo analysis. For the described embodiment, these variables are: tester environment, system environment,

5    system-to-tester offset and reliability wearout mechanisms. Each statistical model will first be described followed by the description of the overall method and system.

Product performance or maximum frequency (FMAX) will be used to describe the invention because it is a critical specification in described embodiment which is built around the testing of integrated circuits, particularly processors. However it should be obvious to those skilled in the

10   art that this methodology could be applied to other product specification such as but not limited to: the minimum / maximum operating voltage of a product, the minimum / maximum operating temperature of a product, minimum / maximum operating power of a product, minimum / maximum sleep mode power of a product, access time for memory products, or any key product specification.

15   For processors, FMAX, the maximum frequency that the integrated circuit will operate in the system environment, is important in terms of the application and price at which the processor will be sold. As a result of process variation, each processor has a different FMAX. Measuring FMAX and sorting a processor by performance is accomplished by running a set of functional test patterns at the desired sort frequencies. A processor is binned at the highest sort frequency in

20   which all patterns function. Generally, the FMAX of the processor as measured on a tester is faster than the FMAX of the processor as measured in a system.

The tester environment is one input to the guardband model. Tester characterization involves quantifying those variables that may contribute to inaccuracies in a product specification (i.e. FMAX) measurement on a tester. These include contributions such as: tester timing

25   accuracy, clock edge placement accuracy, power supply distribution, temperature distribution and tester-to-tester offset. The error in FMAX can be broken up into two components, one mechanical and one electrical. The mechanical component contains the DIB (device under test interface board) and handler, and the electrical component focuses on the pin electronics of the tester. Both components add to the inaccuracy in the FMAX measurement. The FMAX errors

30   are then characterized, and a model is developed using a statistical programming tool. SAS by SAS Institute, Inc., a commercially available statistical programming tool, is suitable for such use, but other programs could be used as well (i.e. MATLAB by Mathworks, Inc., MATHCAD by MathSoft, Inc.,etc.).

35

System environment characterization involves quantifying those variables that may contribute to inaccuracies or anomalies in a product specification (i.e. FMAX) in a system. These include such application conditions as compatibility with different components, assessing effects of manufacturing process variation, temperature variation, power supply variation and

5 noise margin.

In FIG. 3 the process for obtaining the model for the system environment is illustrated. In order to obtain the data for this characterization various system environments are setup at step 21 for product measurements. A typical setup would include a means of varying system frequency (i.e. external oscillator), a means of varying power supply voltage (i.e. voltage regulator),

10 temperature controller (i.e. Peltier device) and a means of inserting various samples into the same board (i.e. a socket). Since not all parts run at their specified voltage/temperature, system power supply and temperature are statistically modeled at step 23 using various samples under normal operating conditions. These models provide a means of predicting a particular voltage and temperature value for any given processor operating at any given time. Next at step 25, the

15 system is initialized (desired operating temperature, voltage and PLL mode are selected). The variable oscillator is then set to a low value and at step 27 the processor is booted at a slow frequency. At step 29 the frequency of the oscillator is increased in fixed intervals until the system no longer boots. The processor is rebooted at the frequency the system hanged. If the system boots, it is exercised using an intensive and comprehensive suite of software packages. If the

20 processor could not run the complete software suit successfully, the oscillator frequency is lowered at step 35 until the processor boots and the software verification testing at step 31 is repeated. If the processor booted and ran all software without hanging, the FMAX is recorded at step 33. This process is repeated at step 37 for another voltage, temperature, PLL mode or processor. When process is complete, the FMAX data for the system environment are

25 characterized at step 39 and included with the tester models.

Once product FMAX data is collected on a given number of integrated circuits, both on a tester and in a system, that data can be analyzed to determine the system-to-tester offset model. Based on various products studied, in gathering system and tester data best results occur by sampling at least 15 to 20 processors per performance sort generated. At step 50 the system and

30 tester FMAX data is input into the statistical software program. At step 52 a system-to-tester FMAX delta is calculated. This delta at step 54 is tested for best distribution type (typically, the distribution is Gaussian). Based on best distribution fit, at step 58 distribution parameters are calculated based on sample size and confidence selected at step 60 (for Gaussian distribution, population mean and standard deviation are estimated). For a Gaussian distribution, a

35 t-distribution is used to estimate population mean and chi-squared distribution is used to estimate population standard deviation. These results are output to the Monte Carlo routine at step 62.

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This process is repeated through step 64 for each performance sort or system under analysis until process is completed at step 66.

Reliability wearout mechanisms are estimated using both technology models and product specific data ( power on hours, use voltage, use temperature, etc.). Depending on the wearout

5 mechanism, different parameters will drive guardband. In the case of processor's hot electron (hot-e) degradation is an important specification. However, this technique could be extended to cover other reliability wearout mechanisms (i.e. SER, electromigration, etc.). A hot-e guardband model is developed using technology models (design manual equations, circuit models, etc.) and product specific variables such as operating voltage, operating temperature and average channel

10 length per speed sort. This model predicts performance degradation at end of life. Hot-e is primarily driven by high voltage and short channel length. As illustrated in FIG. 6 fail rates increase on axis 15 with frequency (shorter channel lengths) and on axis 13 with voltage. This reliability data is characterized by the statistical software program to form a reliability model.

As illustrated in FIG. 7 the models previously described denoted as blocks 110, 120, and

15 130 are inputs to the Monte Carlo analysis as well as market sector quality (i.e. SPQL) expectations denoted as block 140. Each model is incorporated using the distribution type determined during the analysis previously described. A loop value is set (shown as 10,000, in block 150 but can be any relatively large number). Each model contributes a value at step 160 which is randomly selected based on distribution type. One guardband value is determined by

20 combining the individual values and then adding hot-e input based on performance sort. This is repeated through steps 180, 190 and 170 until the loop value selected in block 150 is reached. The output is a distribution of guardbands based on all factors previously discussed. Finally, depending on market quality expectations input at block 200, a guardband can be selected at 210 which intelligently satisfies market tolerance expectations while minimizing yield loss (See Figure

25 2). As can be seen from Fig. 2, trimming a few percent off a guardband , shown as vertical axis 4, to make yield targets without understanding the effects on product quality may adversely effect product quality. The opposite holds true as well. Over-guardbanding can lead to quality levels not required in the market which can in turn adversely affect yields and revenue.

As mentioned earlier any statistical software program can be used with the invention. SAS

30 is used in the current implementation, but other programs are just as good (i.e. MATLAB, MATHCAD, etc.). One also uses these statistical software programs when determining the "critical specification" probability statistics. You also use the statistical software for running the Monte Carlo analysis for determining the final guardband.

35

FIG. 8. illustrates the typical hardware configuration of a computer system capable of creating the test guardband in accordance with the subject invention. The configuration comprises at least one processor or central processing unit (CPU) 10. CPU(s) 10 is interconnected via system bus 12 to a random access memory (RAM) 14, read-only memory

5   (ROM) 16, an input/output (I/O) adapter 18 for connecting peripheral devices such as disk units 20 and tape drives 40 containing a statistical program capable of doing statistical distribution analysis to bus 12, user interface adapter 22 for connecting keyboard 24, mouse 26, speaker 28, microphone 32, and/or other user interface devices such as touch screen device (not shown) to bus 12 for inputting data such as tolerance data, communication adapter 34 for connecting the

10  information handling system to a data processing network and for inputting various environmental models into the computer the models, and display adapter 36 for connecting bus 12 to display device 38. The variable inputs shown on FIG. 7 and the SAS software are loaded on the appropriate disk or tape units or fed either through I/O adapters or the network for processing. A computer program with an appropriate application interface could be created by

15  one of skill in the art and stored on the system to simplify the practicing of this invention.

Although this disclosure identifies a preferred embodiment, it should be noted this system could be easily extended to enable quantifiable business decisions which maximize revenue while not sacrificing quality when considering variables that affect products or process specifications by: implementing other analysis methods, including other variables that affect maximizing revenue

20  while balancing risk and also applying this system to other applications within and outside the semiconductor industry.

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## Claims

1.  A method for determining a specification guardband comprising the steps of:

5   creating a set of distribution models representative of variables that affect said specification;

analyzing the set of models with a statistical tool that can work with the distribution models; and

selecting a guardband for said specification based on the statistical analysis and a tolerance target
10  for the said specification under analysis.


2.  The method of claim 1 where one of the variables is the system on which the product is used.

15
3.  The method of claim 2 where one of the variables is the system to tester offset.


4. The method of claim 1 where one of the variables is the test system which the guardband is
20  used.


5.  The method of claim 1 where the statistical tool uses a Monte Carlo analysis.

25
6.  The method of claim 1 where the product specification is maximum frequency.


7.  The method of claim 1 where a sample chosen for creating the models is at least 10.
30

8.  The method of claim 1 where the tolerance target is a quality target.


35 9. The method of claim 1 where the tolerance target is a revenue target.


10.  The method of claim 1 where one of the set of models is a reliability wearout model.

40
11.  The method of claim 1 where student-t and chi-squared distribution models are used.

12. The method of claim 2 where the step of creating a set of models includes the additional steps of:

setting up the system environment;

modeling system variables distributions during normal operation;

setting initial system variables;

booting the system at increasing frequencies until the system hangs;

running system applications at the highest frequency at which the system functions and record such frequency; and

changing the initial system variables and performing on the new variables the same steps applied to the initial system variables.

13. The method of claim 3 where the creating a set of models includes the additional steps of:

inputting tester to system correlation data;

calculating system to tester offset for a set of samples;

choosing an appropriate distribution model for the tester to system offset and

calculating a tester to system mean and sigma based on the sample size.

14. The method of claim 4 where the step of creating a set of models includes the additional steps of:

characterizing tester system electrical and mechanical parameters that affect specifications under analysis;

characterizing tester system to tester system offset;

choosing an appropriate distribution model for said tester system parameters; and

tester system offset.

15. The method of claim 12 where system variable distributions are power supply voltage and operating temperature.

5  16. The method of claim 12 where the method of calculating tester to system mean and sigma is applied to a different speed sort.

17. The method of claim 13 where the method of calculating tester to system mean and sigma is 10 applied to a different system.

18. The method of claim 14 where tester system electrical parameters are tester timing accuracy, clock edge placement accuracy and tester power supply distributions.
15

19. The method of claim 14 where tester system mechanical parameters are device under test interface board, tester temperature and tester handler distributions.

20

20. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, the method comprising the steps of:

25 creating a set of distribution models representative of environmental variables for the tester and the product under test, the set of models based on a product parameter variables that affect said specification;

analyzing the set of models with a statistical tool that can work with the distribution models; and
30

selecting a guardband for the tester said specification based on the statistical analysis and a tolerance target for the product under test said specification under analysis.

35 21. The program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, of claim 20 wherein the program of instruction provides that one of the variables is the system on which the product is used.

40
22. The program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, of claim 20 wherein the program of instruction provides that one of the variables the system to tester offset.

45

23. The program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, of claim 20 wherein the program of instruction provides that one of the variables is test system where the guardband is used.

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24. The program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, of claim 20 wherein the program of instruction provides that one of the set of models is a reliability wearout model.

10

25. The program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, of claim 20 wherein the program of instruction includes statistical program tool that uses a Monte Carlo analysis.

15

26. The program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for determining a tester guardband, of claim 20 wherein the program of instruction provides that the models are student-t and chi-squared distribution models

20

25 27.. A computer configured for determining a tester guardband, the computer comprising:

an application interface for inputting various environmental models into the computer the models comprising a tester model and system model;

30 a memory that contains a statistical program capable of doing statistical distribution analysis;

an application interface for inputting tolerance data;

an execution unit that receives the statistical program and environmental models and processes the
35 guardbands based on the tolerance data; and

an I/O device for outputting the guardband data ..

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# STATISTICAL GUARDBAND METHODOLOGY

## ABSTRACT

A method for creating a guardband that incorporates statistical models for test environment, system environment, tester-to-system offset and reliability into a model and then processes a final guardband by factoring manufacturing process variation and quality against yield loss.
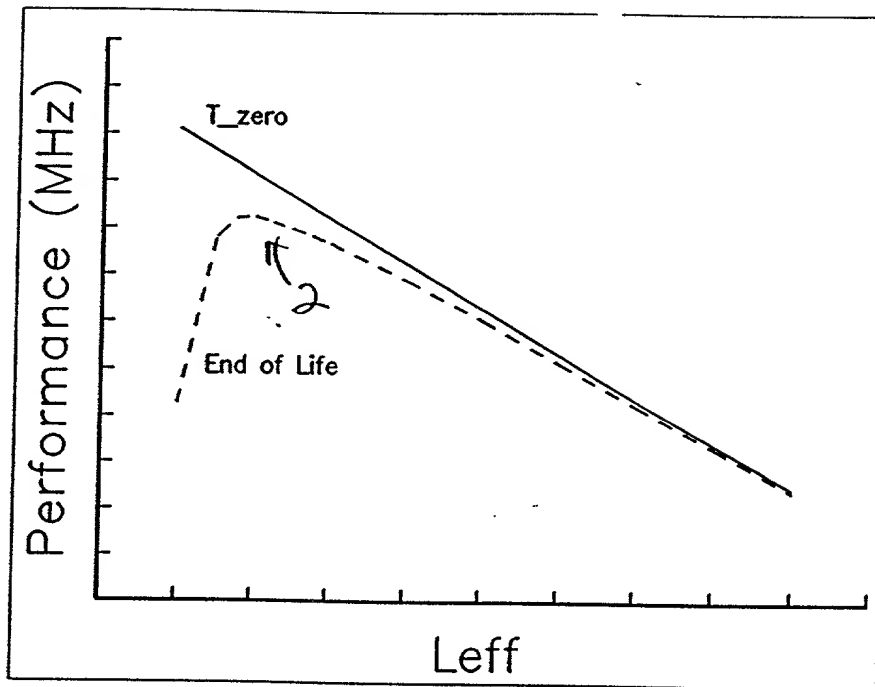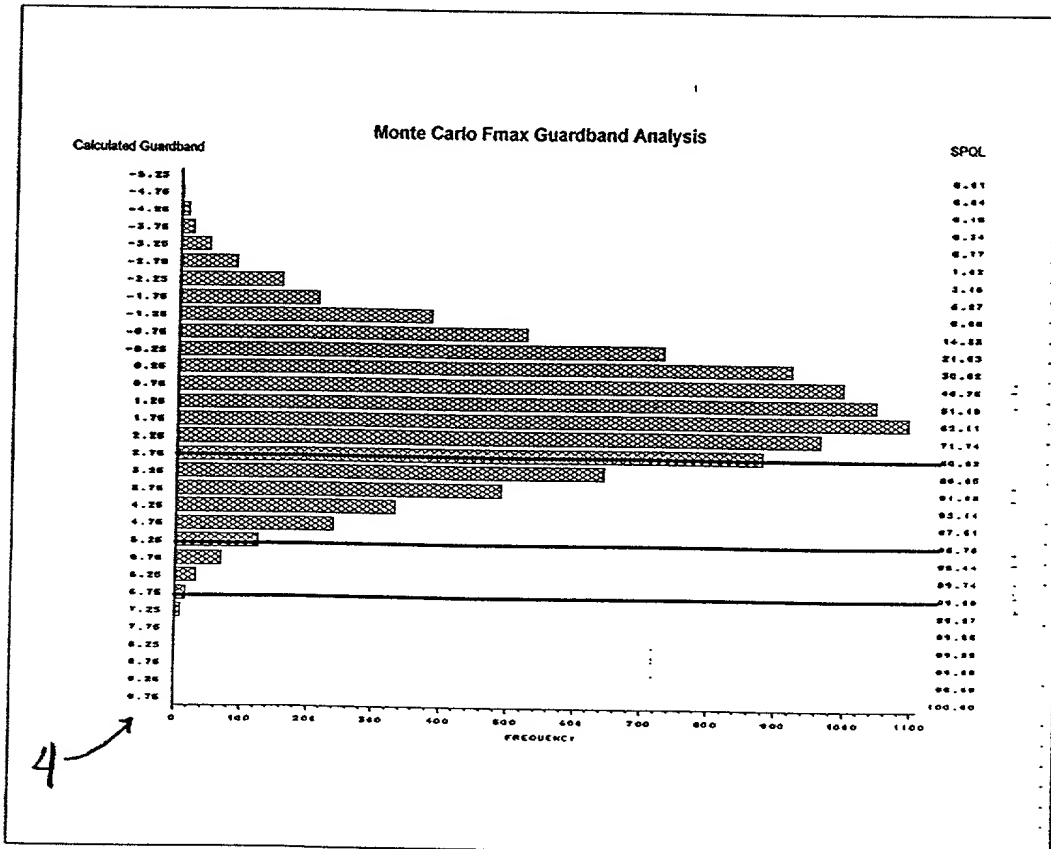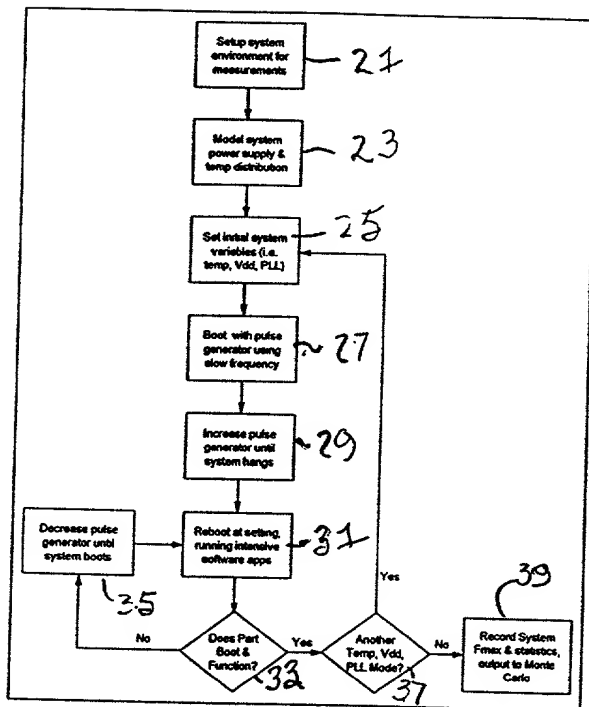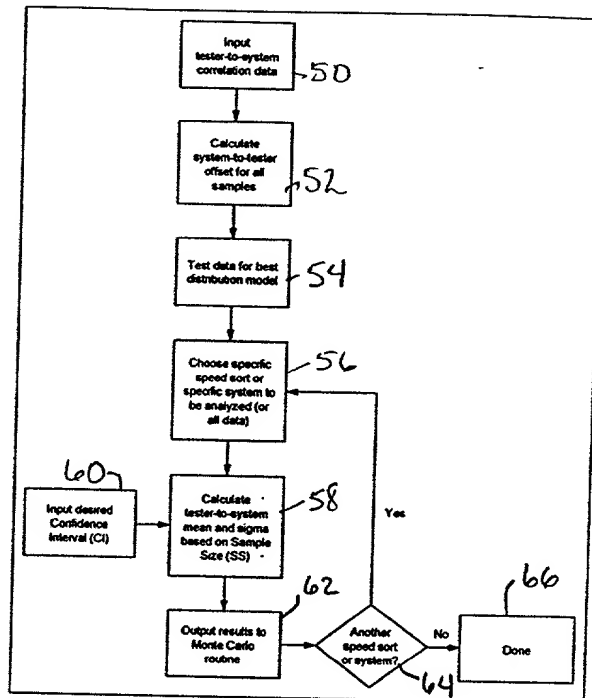
5

Figure 1.



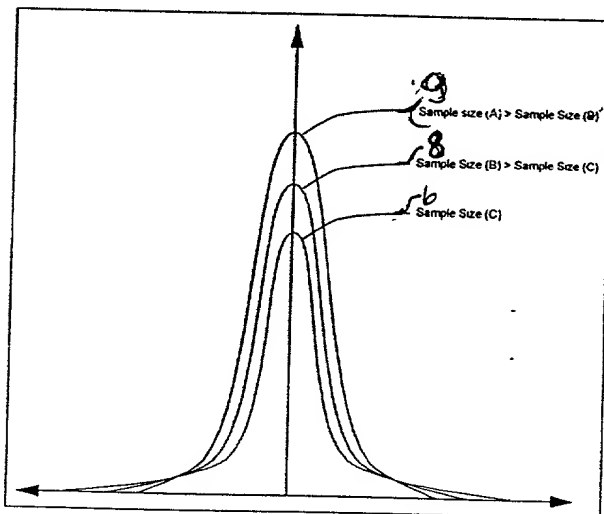Figure 2.

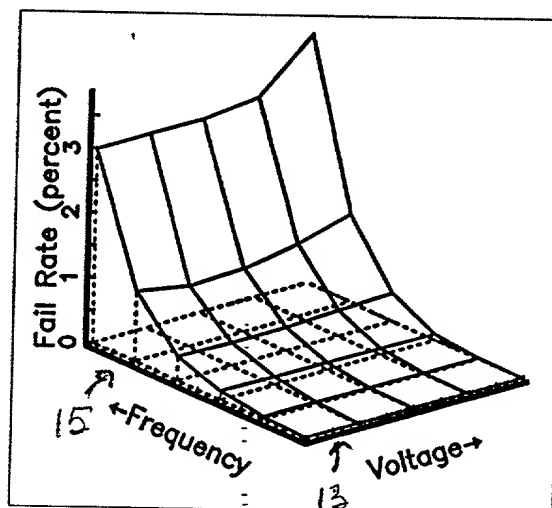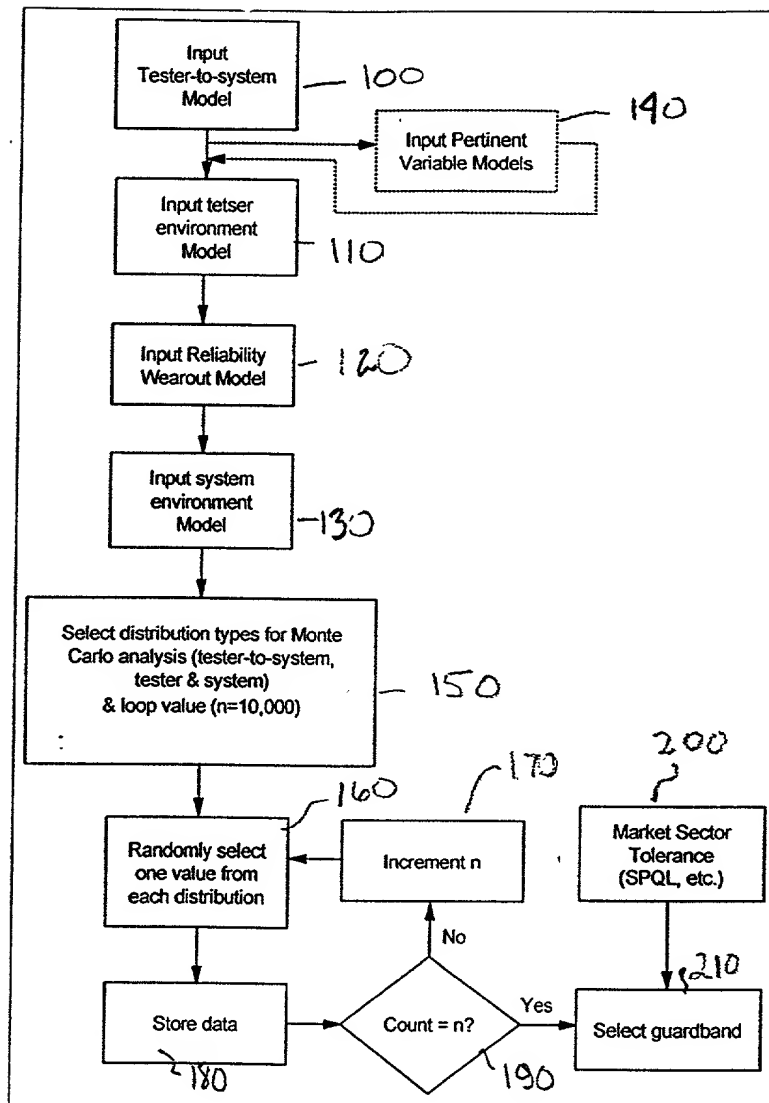Figure 3.



Figure 4.



Figure 5.
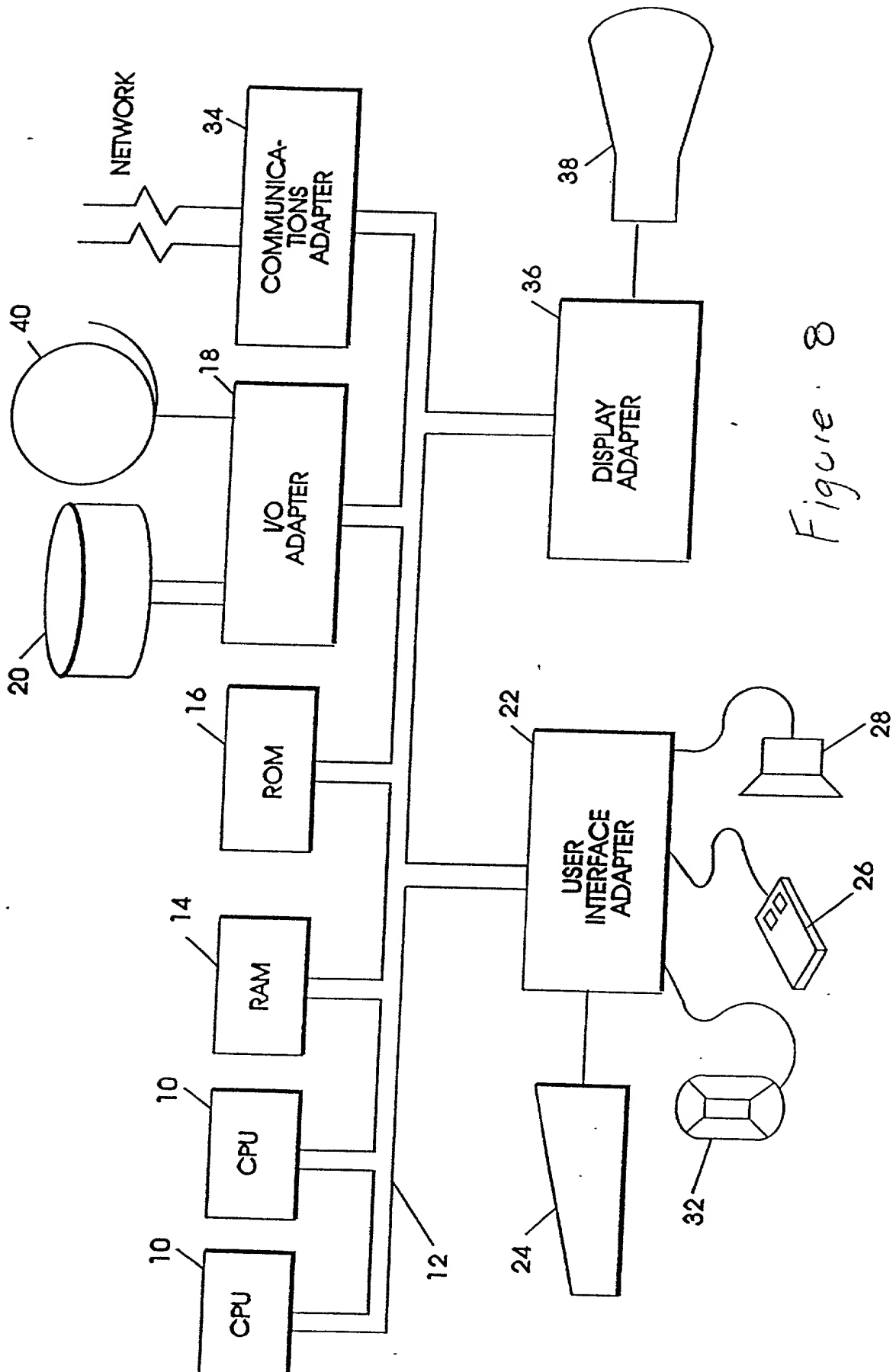


Figure 6.

Figure 7.

Figure 8

# Declaration and Power of Attorney for Patent Application

As a below named inventor, I hereby declare that::

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

### STATISTICAL GUARDBAND METHODOLOGY

the specification of which (check one)

| X | is attached hereto. |

| | was filed on _____ as Application Serial No _____ and was amended on _____ |

—.

I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

| Number | Country | Day/Month/Year | Priority Claimed |
|--------|---------|----------------|------------------|

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications.

| Serial No. | Filing Date | Status |
|-----------|-------------|--------|
| 60/172,198 | 12/17/99 | Pending |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: **Mark F. Chadurjian, Reg. No. 30,739; Richard A. Henkler, Reg. No. 39,220; Richard M. Kotulak, Reg. No. 27,712; James M. Leas, Reg. No. 34,372; William D. Sabo, Reg. No. 27,465; Eugene I. Shkurko, Reg. No. 36,678; Robert A. Walsh, Reg. No. 26,516 and Howard J. Walter, Jr., Reg. No. 24,832; Christopher A. Hughes, Reg. No. 26,914; Edward A. Pennington, Reg. No. 32,588; John E. Hoel, Reg. No. 26,279; Joseph C. Redmond, Jr., Reg. No. 18,753.**

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---

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                                                                        Date

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---

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Post Office
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**Page 2 of 3**

(5)　Inventor:　Michael D. Maurice

Signature: _____　　03/02/00
　　　　　　　　　　　　　　　　　　　　　　　　　Date

Residence:　8 Garbaree Lane, Jericho, Vermont 05465

Citizenship:　United States of America

Post Office
Address:　　Same as residence

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(6)　Inventor:　Timothy J. O'Gorman

Signature: _____　　3/7/00
　　　　　　　　　　　　　　　　　　　　　　　　　Date

Residence: 248 Lefebvre Lane, Williston, Vermont 05495

Citizenship: United States of America

Post Office
Address:　　Same as residence

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(7)　Inventor:　Regis D. Parent

Signature: _____　　03/01/00
　　　　　　　　　　　　　　　　　　　　　　　　　Date

Residence: 83 Bill Cook Road, Underhill, Vermont 05489

Citizenship: Canada

Post Office
Address:　　Same as residence

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(8)　Inventor:　Jeffrey S. Zimmerman

Signature: _____　　03/02/00
　　　　　　　　　　　　　　　　　　　　　　　　　Date

Residence: 123 Hemlock Hill Road, Hinesburg, Vermont 05461

Citizenship: United States of America

Post Office
Address:　　Same as residence